

# **Enhanced Serial Peripheral Interface (eSPI) ECN**

#### **Engineering Change Notice**

TITLE	Clarify Flash Erase Length field for MAFS and SAFS			
DATE	May 2020			
AFFECTED DOCUMENT	eSPI Base Specification (Revision 1.0) eSPI Addendum for Server Platforms (Revision 0.7)			
DISCLOSURE RESTRICTIONS	CNDA or eSPI Click to Accept License Agreement			



Intel hereby grants you a fully-paid, non-exclusive, non-transferable, worldwide, limited license (without the right to sublicense), under its copyrights to view, download, and reproduce the Enhanced Serial Peripheral Interface (eSPI) Specification ("Specification"). You are not granted any other rights or licenses, by implication, estoppel, or otherwise, and you may not create any derivative works of the Specification.

The Specification is provided "as is," and Intel makes no representations or warranties, express or implied, including warranties of merchantability, fitness for a particular purpose, non-infringement, or title. Intel is not liable for any direct, indirect, special, incidental, or consequential damages arising out of any use of the Specification, or its performance or implementation.

Intel retains ownership of all of its intellectual property rights in the Specification and retains the right to make changes to the Specification at any time. No license is granted to use Intel's name, trademarks, or patents.

If you provide feedback or suggestions on the Specification, you grant Intel a perpetual, non-terminable, fully-paid, nonexclusive, worldwide license, with the right to sublicense, under all applicable intellectual property rights to use the feedback and suggestions, without any notice, consent, or accounting. You represent and warrant that you own, or have sufficient rights from the owner of, the feedback and suggestions, and the intellectual property rights in them, to grant the above license.

This agreement is governed by Delaware law, without reference to choice of law principles. Any disputes relating to this agreement must be resolved in the federal or state courts in Delaware and you consent, and will not object, to the exclusive personal jurisdiction of the courts in Delaware.

This agreement is the entire agreement of the parties regarding the Specification and supersedes all prior agreements or representations.

This agreement is hosted at the following location: <a href="http://downloadcenter.intel.com/Detail">http://downloadcenter.intel.com/Detail</a> <a href="Desc.aspx?agr=Y&DwnldID=21353">Desc.aspx?agr=Y&DwnldID=21353</a>

THIS SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE.

Except for a limited copyright license to copy this specification for internal use only, no license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

Intel Corporation and the authors of this specification disclaim all liability, including liability for infringements of proprietary rights, relating to implementation of information in this document and the specification. Intel Corporation and the authors of this specification also do not warrant or represent that such implementation(s) will not infringe such rights.

Implementations developed using the information provided in this specification may infringe the patent rights of various parties including the parties involved in the development of this specification. Except as expressly granted hereunder, no license, express or implied, by estoppel or otherwise, to any intellectual property rights (including without limitation rights under any party's patents) is granted.

All suggestions or feedback related to this specification become the property of Intel Corporation upon submission.

Intel may make changes to the specifications, product descriptions, and plans at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

This document is an intermediate draft for comment only and is subject to change without notice. Do not finalize a design based on this document.

Intel and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

 $\boldsymbol{\ast}$  Other names and brands may be claimed as the property of others.

Copyright 2020, Intel Corporation. All rights reserved.



# **ECN Motivation**

The eSPI Base Specification (revision 1.0) and the eSPI Addendum for Server Platforms (revision 0.7) describe the Erase command length.

The feedback received is driving this spec clarification related to Erase command length. This ECN provides clarity on the Flash Erase Length field for both MAFS and SAFS.

**Note**: Refer to the EDS and PDG of the relevant platforms for details on SAFS support.

eSPI Base Specification (revision 1.0) describes the following related to the Flash Erase command Length field:

- Section 5.1.3 Length
   For Flash Erase, the least significant 3 bits of the length field specifies the size of the block to be erased with the encoding matches the value of the Flash
   Block Erase Size field of the Channel Capabilities and Configuration register.
- Section 5.2.4.1 Master Attached Flash Sharing
   The Address field specifies the beginning of the erase block and the least significant 3 bits of the length field specifies the size of the block to be erased.
   The encoding of the least significant 3 bits of the length field matches the value of the Flash Block Erase Size field of the Channel Capabilities and Configuration register.
- Section 7.2.1.7 Offset 40h: Channel 3 Capabilities and Configurations

Bit	Туре	Default	Description			
4:2	RW	01b	Flash Block Erase Size: eSPI master sets this field to communicate the block erase size to the slave.  This field is applicable only to master attached flash sharing scheme.  000b: Reserved 001b: 4 Kbytes 010b: 64 Kbytes 011b: Both 4 Kbytes and 64 Kbytes are supported 100b: 128 Kbytes 101b: 256 Kbytes 110b - 111b: Reserved			

On the other hand, eSPI Addendum for Server Platforms (Revision 0.7) defines the following related to Flash Erase Length field:

Section 2.6 – Slave Attached Flash Sharing Operation
 The Address and Length fields ({Length1[3:0], Length0[7:0]}) of the standard eSPI packet format will have the definitions as specified in Table 2 7. The



Length field will specify the length of the write data to the flash device or requested size of the read data from the flash device (as described in the eSPI Base Specification). The only exception will be for the flash erase block sizes, where the length encodings are as listed in Table 2-7.

Section 2.1.2 – Offset 44h: Channel 3 Capabilities and Configurations 2

Bit	Туре	Default	Description		
			Target Flash Erase Block Size for Master's Regions: This field indicates the sizes of the erase commands the master may issue. If multiple bits are set then the maste may issue an erase using any of the indicated sizes.		
			If multiple regions are accessible by the master, this field advertises the common erase block sizes for these regions.		
			This field is only applicable when slave attached flash sharing scheme is selected.		
15:8	RO	HwInit			
			Bit 0: 1 Kbytes EBS supported		
			Bit 1: 2 Kbytes EBS supported		
			Bit 2: 4 Kbytes EBS supported		
			Bit 3: 8 Kbytes EBS supported		
			Bit 4: 16 Kbytes EBS supported		
			Bit 5: 32 Kbytes EBS supported		
			Bit 6: 64 Kbytes EBS supported		
			Bit 7: 128 Kbytes EBS supported		

• Table 2.7 – eSPI Flash Access Channel Packet Format for Master and Slave Attached Flash Configurations

Table 2-7. eSPI Flash Access Channel Packet Format for Master and Slave Attached Flash Configurations

Cycle Type [7:0]	Flash Command Type	Flash Operation	Address Size	Length [11:0] (3)	Slave Attached Flash Supported	Master Attached Flash Supported
02h	Standard	Erase	4 B	0h: 4 KB 1h: 32 KB 2h: 64 KB	Yes (1)	Yes (1)
				3h - FFFh: Reserved		

Due to conflicting description related to Flash Erase Length field, this ECN therefore clarifies the Flash Erase Length field for both MAFS and SAFS:

For Master Attached Flash Sharing (MAFS), the least significant 3 bits of the Flash Erase Length field specifies the size of the block to be erased with the encoding matches the value of the Flash Block Erase Size field of the Channel Capabilities and Configuration register. However, length field encoding of "011" is not applicable for Flash Erase in MAFS.



 For Slave Attached Flash Sharing (SAFS), the Flash Erase Length field encoding is as defined in Table 2.7. For consistency with Table 2.7, Block Erase Size of 1KB, 2KB, 8KB and 16KB for SAFS are deprecated (reserved) in the Slave register.



# **ECN Description**

Changes (as highlighted) to the eSPI Base Specification:

#### **5.1.3** Length

For Flash Erase, the least significant 3 bits of the length field specifies the size of the block to be erased with the encoding matches the value of the Flash Block Erase Size field of the Channel Capabilities and Configuration register.

For Flash Erase length field definition, refer to the Master Attached Flash Sharing (MAFS), and Slave Attached Flash Sharing (SAFS) section for detail.

#### **5.2.4.1 Master Attached Flash Sharing**

Flash Erase is a non-posted request with no data. This command instructs the SPI Flash controller to erase a part of the region allocated to the eSPI slave. The Address field specifies the beginning of the erase block and the least significant 3 bits of the length field specifies the size of the block to be erased. The encoding of the least significant 3 bits of the length field matches the value of the Flash Block Erase Size field of the Channel Capabilities and Configuration register. The specified address must be aligned to the block erase size. The supported erase block size is programmable and is communicated by the eSPI master to the slave through the Channel Capabilities and Configuration register. However, length field encoding of "011" is not applicable for Flash Erase in Master Attached Flash Sharing (MAFS).



Changes (as highlighted) to eSPI Addendum for Server Platforms:

### 2.1.2 Offset 44h: Channel 3 Capabilities and Configurations 2

Bit	Туре	Default	Description		
			Target Flash Erase Block Size for Master's Regions: This field indicates the sizes of the erase commands the master may issue. If multiple bits are set then the master may issue an erase using any of the indicated sizes.		
			If multiple regions are accessible by the master, this field advertises the common erase block sizes for these regions.		
			This field is only applicable when slave attached flash sharing scheme is selected.		
15:8	RO	HwInit			
			Bit 0: Reserved <del>1 Kbytes EBS supported</del>		
			Bit 1: Reserved <del>2 Kbytes EBS supported</del>		
			Bit 2: 4 Kbytes EBS supported		
			Bit 3: Reserved 8 Kbytes EBS supported		
			Bit 4: Reserved <del>16 Kbytes EBS supported</del>		
			Bit 5: 32 Kbytes EBS supported		
			Bit 6: 64 Kbytes EBS supported		
			Bit 7: 128 Kbytes EBS supported		

## 2.6 Slave Attached Flash Sharing Operation

Table 1-7. eSPI Flash Access Channel Packet Format for Master and Slave Attached Flash Configurations

Cycle Type [7:0]	Flash Command Type	Flash Operation	Address Size	Length [11:0] (3)	Slave Attached Flash Supported	Master Attached Flash Supported
02h	Standard	Erase	4 B	MAFS:  Oh: Reserved  1h: 4 KB  2h: 64 KB  3h: Reserved  4h: 128 KB  5h: 256 KB  6h - FFFh: Reserved  SAFS:  Oh: 4 KB  1h: 32 KB  2h: 64 KB  3h: 128 KB  4h - FFFh: Reserved	Yes (1)	Yes (1)

