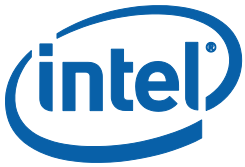

Enhanced Serial Peripheral Interface (eSPI) ECN

Engineering Change Notice

TITLE	Support for Host & CPU to access an BMC integrated RTC
DATE	11 July 2020
AFFECTED DOCUMENT	eSPI Base Specification (Revision 1.0) eSPI Addendum for Server Platforms (Revision 0.7)
DISCLOSURE RESTRICTIONS	CNDA or eSPI Click to Accept License Agreement

ECN Motivation

As the manufacturing process is optimize, integrating a real time clock (RTC) on Intel's silicon will no longer be possible on future platform generations. The RTC clock and the RTC RAM content cannot be active for an extended length of time (which varies per platform segment, between 180 days to 7 years), due to the reduction of number of nodes on the optimize manufacturing process.

The eSPI Base Specification (revision 1.0) describes bit 29 of the General Capabilities and Configuration register (offset 08h) as reserved. This ECN provides a description and details of this bit 29 update.

ECN Description

Intel's next generation platforms facilitates the use of the RTC in the Baseboard Management Controller (BMC).

Note: consult with your BMC vendor of choice about support for the following bit configuration update.

Current eSPI Base Specification (revision 1.0):

7.2.1.3 Offset 08h: General Capabilities and Configurations

This register is also reset by the In-band RESET command.

Bit	Type	Default	Description
29	RO	0	**Reserved.**

Update to eSPI Base Specification (revision 1.0):

eSPI master will read bit[29] of the general capabilities and configurations register (offset 0x8).

Offset 08h: General Capabilities and Configurations

Bit	Type	Default	Description
29	RO	0	**RTC-integrated-BMC** **1:** BMC supports an integrated RTC to which eSPI master can forward RTC targeting IO cycles **0:** BMC does not support an integrated RTC

When bit 29 is set (1), RTC cycles are sent downstream as IO Read or IO Write cycles. Please see platform specific eSPI compatibility spec for more details.

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