



Intel® Desktop Board 845GL Chipset Family Specification Update

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Order Number: A98269-009

Intel® Desktop Boards using the Intel® 845GL chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update and its companion document, the Intel® Desktop Board Product Supplement Specification Update.

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The Intel® desktop boards using the Intel® 845GL chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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REVISION HISTORY

Date of Revision	Version	Description
June 2002	-001	This document is the first Specification Update for Intel® Desktop Boards using the Intel® 845GL chipset. Added Document Changes 1 and 2.
August 2002	-002	Added Specification Change 1.
September 2002	-003	Added Erratum 1. Removed Printed Board Assembly (PBA) information from the document, as this reference is no longer valid. Updated the Legal Disclaimer Section.
October 2002	-004	Added Specification Changes 2, 3. Added Erratum 2.
February 2003	-005	Moved Specification Changes 4-8 from the <i>Intel® Desktop Board D845GLAD Product Supplement Document</i> (Order number A98273). Added Errata 3. Added Specification Clarification 1.
March 2003	-006	Added Erratum 4. Added Documentation Changes 3, 4.
April 2003	-007	Added Documentation Change 5.
July 2003	-008	Added Specification Change 9.
November 2003	-009	Added Specification Clarification 2.



PREFACE

This document is an update to the specifications contained in the *Technical Product Specification for Intel® Desktop Boards using the 845GL Chipset* (Order number A90788). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Intel® Pentium® 4 Processor Specification Update* (Order number 249199) for specification updates concerning the Intel Pentium 4 processor and that may apply to the Intel® Desktop Board 845GL chipset family. Unless otherwise noted in this document, it should be assumed that any processor errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Refer to the *Intel® 845 Chipset: 82845 Memory Controller Hub (MCH) Specification Update* (Order Number 298589) for specification updates concerning the 82845GL MCH Controller and that may apply to the Intel® Desktop Board 845GL chipset family. Unless otherwise noted in this document, it should be assumed that any MCH errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Specification Update* (Order Number 290745) for specification updates concerning the 82801 I/O Controller Hub and that may apply to the Intel® Desktop Board 845GL chipset family. Unless otherwise noted in this document, it should be assumed that any 82801DB I/O Controller Hub (ICH) errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause desktop boards using the Intel® 845GL chipset's behavior to deviate from published specifications. Hardware and software designed to be used with any given Altered Assembly (AA) and BIOS revision level must assume that all errata documented for that AA and BIOS revision level are present on all desktop boards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

**Specification Update for
Intel® Desktop Boards Using the Intel® 845GL Chipset**



GENERAL INFORMATION

Information contained in the *Specification Update for Intel® Desktop Boards using the Intel® 845GL Chipset* is intended to be used with *Product Supplement Specification Update* documents (available separately).

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to desktop boards using the Intel® 845GL chipset. Intel intends to fix some of the errata in a future revision of the desktop board, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future revision of the desktop board, driver, or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Change to description of Section 1.11.1, Fan Monitoring
2	Doc	Change to section 1.11.2, Chassis Intrusion
3	Doc	Addition to section 4.5, Security Menu BIOS setup options
4	Doc	Change to description of Section 1.4, Board Layout
5	Doc	Change to description of Section 2.2, Connectors
6	Doc	Change To Description of Section 2.2.2.2, Audio, Power, And Hardware Control Connectors
7	Doc	Addition of Table 5A, Front Panel Audio Connector
8	Doc	Change to description of Section 2.3, Jumper Block
9	Doc	Change to Section 4.3, Main Menu, BIOS Setup Program
NO.	PLANS	ERRATA
1	Fixed	Intel® 82801DB I/O Controller Hub 4 (ICH 4) Erratum 7
2	Fixed	Wake from an ACPI sleep state using wake methodologies may fail
3	PlanFix	Intel 82801DB I/O Controller 4 (ICH 4) Erratum 8
4	PlanFix	Supervisor Password Cleared When 256MB or Greater System Memory is Used
NO.	PLANS	SPECIFICATION CLARIFICATIONS
1	Doc	Addition of Table 4A, Section 2.2.2.2, Audio, Power, and Hardware Control Connectors
2	Doc	Clarification of SMBus routing
NO.	PLANS	DOCUMENTATION CHANGES
1	Doc	Change to Description of Section 3.8.2, Network Boot
2	Doc	Change to description of Section 3.8.4, Changing the Default Boot Device During POST
3	Doc	Removed Note That Specifies USB 2.0 Support Limited to Windows* 2000 and Windows XP From Section 1.7.2, USB



NO.	PLANS	DOCUMENTATION CHANGES (continued)
4	Doc	Removed ESCD Format Reference From Section 3.3.1, PCI Auto configuration
5	Doc	Add Alert Standard Format Specification Version 1.03 Dated June 20, 2001 to Section 1.4, Design Specifications

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *Technical Product Specification for Intel® Desktop Boards using the Intel® 845GL Chipset* (Order Number A90788). All Specification Changes will be incorporated into a future version of that specification.

1. **Change to Description of Section 1.11.1, Fan Monitoring**

Section 1.11.1, Fan Monitoring will change in its entirety as follows:

1.11.1 FAN MONITORING

Fan monitoring can be implemented using Intel® LANDesk Client Manager, or third-party software.

For information about	Refer to
The functions of the fan connectors	Section 1.12.2.2, page 34

2. **Change to Section 1.11.2, Chassis Intrusion**

Section 1.11.2 will change in its entirety as follows:

1.11.2 CHASSIS INTRUSION AND DETECTION

The Desktop Boards support a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed, the mechanical switch is in the closed position.

3. **Addition to Section 4.5, Security Menu BIOS Setup Options**

4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
-------------	------	----------	-----------------	-------	------	------

The menu represented by Table 38 is for setting passwords and security features.

Table 38. Security Menu

Feature	Options	Description
Supervisor Password	No options	Reports if there is a supervisor password set.
User Password	No options	Reports if there is a user password set.

Table 38. Security Menu (cont)

Feature	Options	Description
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
User Access Level (Note 1)	<ul style="list-style-type: none"> • No Access • View Only • Limited • Full (default) 	Sets BIOS Setup Utility access rights for user level.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 2)	<ul style="list-style-type: none"> • Ok (default) • Cancel 	Clears the user password.
Chassis Intrusion	<ul style="list-style-type: none"> • Disabled (default) • Log • Log, notify once • Log, notify til cleared 	<p>Disables Chassis Intrusion Logs the intrusion in the event log Halts system during POST. User must press <F4> to continue. Intrusion flag is cleared and the event log is updated.</p> <p>Halts system during POST. User must enter BIOS setup Security Menu and select "Clear Chassis Intrusion Status" to clear the Chassis intrusion flag.</p>
Clear Chassis Intrusion Status (Note 3)	<ul style="list-style-type: none"> • No Options 	Clears Chassis Intrusion event and updates the Event Log.

Notes:

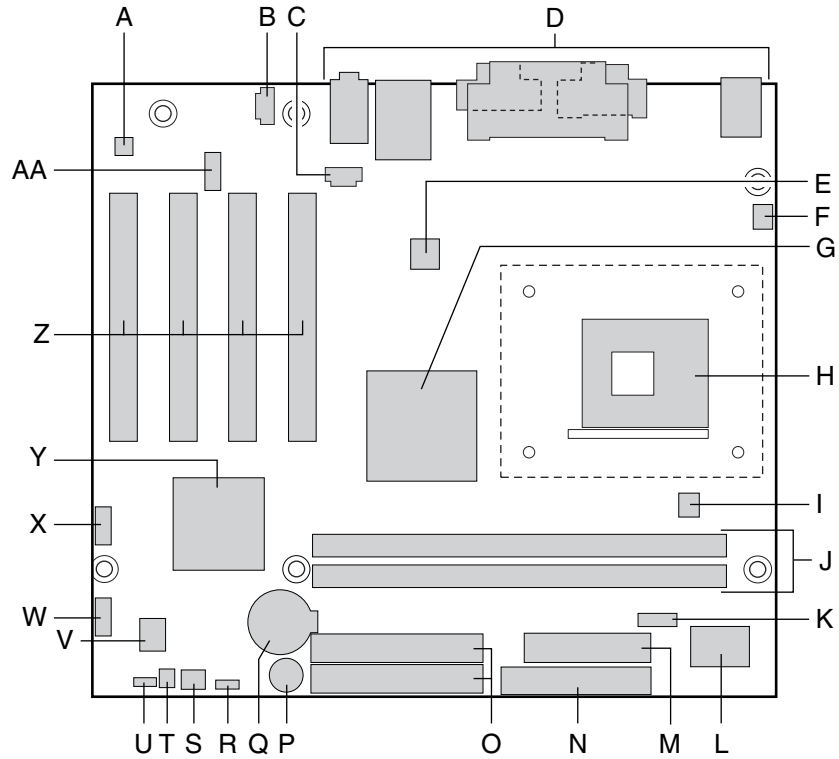
1. This feature appears only if a supervisor password has been set.
2. This feature appears only if a user password has been set.
3. This feature appears only if the Chassis Intrusion log, notify til cleared option has been set.

4. Change to Description of Section 1.4, Board Layout

Section 1.4, Board Layout will change in its entirety as follows:

1.4 Board Layout

Figure 1 shows the location of the major components on the Desktop Board D845GLAD.



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Figure 1 (continued)

A	Audio codec	O	IDE connectors
B	Auxiliary line-in connector	P	Speaker
C	ATAPI CD-ROM connector	Q	Battery
D	Back panel connectors	R	Auxiliary front panel power LED connector
E	+12V power connector (ATX12V)	S	Front chassis fan connector
F	Rear chassis fan connector	T	Chassis intrusion connector
G	Intel® 82845GV Graphics and Memory Controller Hub (GMCH)	U	BIOS Setup configuration jumper block
H	mPGA478 processor socket	V	4 Mbit Firmware Hub (FWH)
I	Processor fan connector	W	Front panel connector
J	DIMM sockets	X	Front panel USB connector
K	Serial port B connector	Y	Intel® 82801DB I/O Controller Hub (ICH4)
L	I/O Controller	Z	PCI bus add-in card connectors
M	Power connector	AA	Front panel audio connector
N	Diskette drive connector		

Figure 1. Desktop Board D845GLAD Components

5. Change to Description of Section 2.2, Connectors

Section 2.2, Connectors will change in its entirety as follows:

2.2 Connectors



CAUTION

Only the back panel USB, front panel USB, VGA, and PS/2 connectors have overcurrent protection. The Desktop Boards' internal connectors are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

This section describes the Desktop Board's connectors. The connectors can be divided into the following groups:

- Back panel I/O connectors (see page 13)
 - PS/2* keyboard and mouse
 - USB
 - Parallel port
 - Serial port
 - VGA
 - LAN (optional)
 - Audio (line out, line in, and mic in)
- Internal I/O connectors (see page 14)
 - Audio (auxiliary line input and ATAPI CD-ROM, and front panel audio)
 - Fans
 - Power
 - Add-in boards (PCI)
 - IDE
 - Diskette drive
 - Chassis intrusion
- External I/O connectors (see page 19)
 - Front panel USB
 - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch, and auxiliary front panel power LED)
 - Auxiliary front panel power/sleep/message-waiting LED

INTEGRATOR'S NOTE

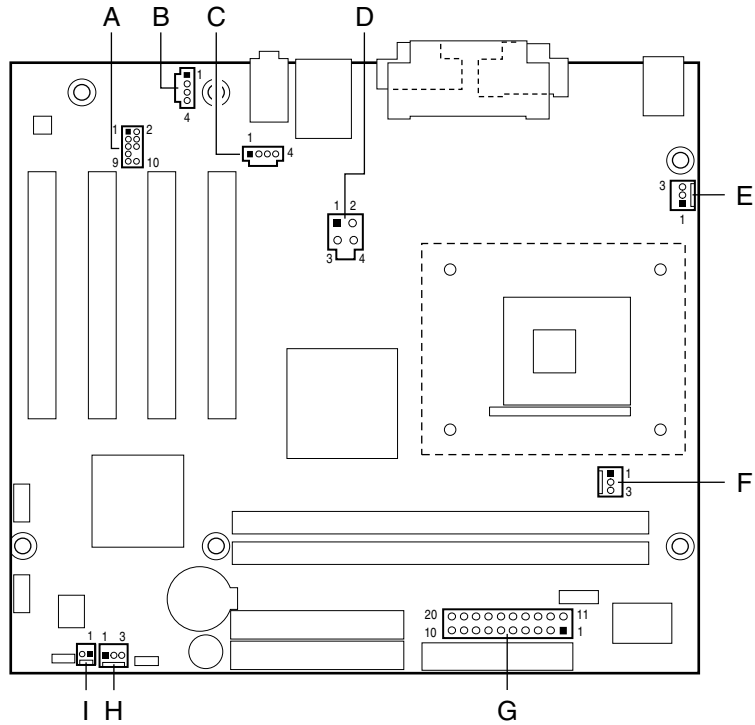
When installing the Desktop Board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, the IDE connector, and the DIMM sockets.

6. Change to Description of Section 2.2.2.2, Audio, Power, and Hardware Control Connectors

Section 2.2.2.2, Audio, Power, and Hardware Control Connectors will change in its entirety as follows:

2.2.2 Audio, Power, and Hardware Control Connectors

Figure 3 shows the location of the audio, power, and hardware control connectors.



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Item	Description	For more information see:
A	Front panel audio	Table 3
B	Auxiliary line in, ATAPI style (white)	Table 4
C	ATAPI CD-ROM (black)	Table 5
D	+12 V power connector (ATX12V)	Table 6
E	Rear chassis fan	Table 7
F	Processor fan	Table 8
G	Main power	Table 9
H	Front chassis fan	Table 10
I	Chassis intrusion	Table 11

Figure 3. Audio, Power, and Hardware Control Connectors

7. Addition of Table 5A, Front Panel Audio Connector

Table 5A Front Panel Audio Connector

Pin	Signal Name	Pin	Signal Name
1	MIC_IN	2	Ground
3	MIC_BIAS	4	+5 V
5	RIGHT_OUT	6	RIGHT_IN
7	Ground	8	Key
9	LEFT_OUT	10	LEFT_IN

NOTE

The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.3 on page 23 for more information.

8. Change to Description of Section 2.3, Jumper Block

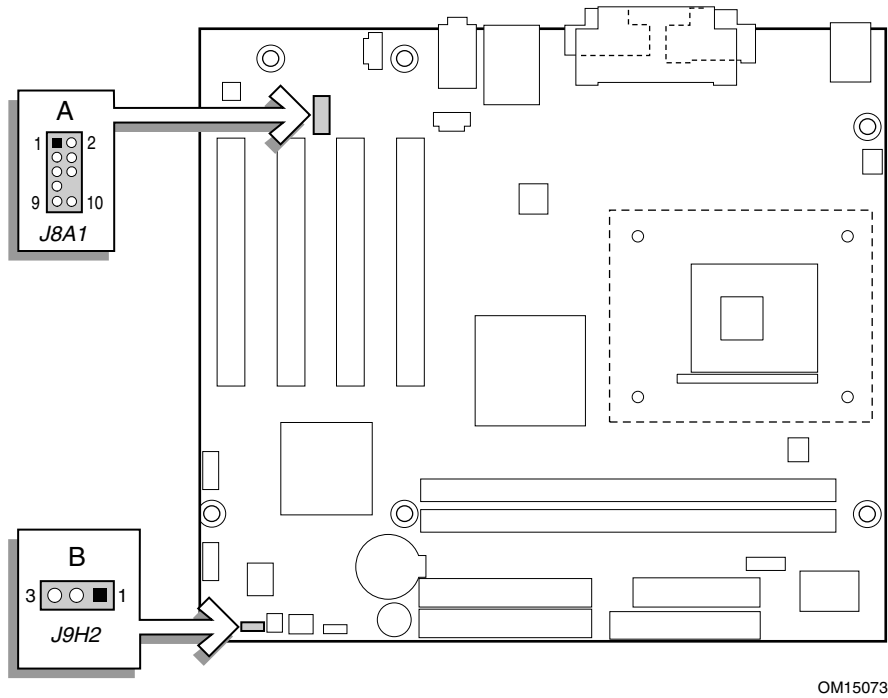
Section 2.3, Jumper Block will change in its entirety as follows:

2.3 Jumper Blocks

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the Desktop Board could be damaged.

Figure 6 shows the location of the jumper blocks.



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Item	Description	Reference Designator
A	Front panel audio connector/jumper block	J8A1
B	BIOS Setup configuration jumper block	J9H2

Figure 6. Location of the Jumper Blocks

2.3.1 FRONT PANEL AUDIO CONNECTOR/JUMPER BLOCK

This connector has two functions:

- With jumpers installed, the audio line out signals are routed to the back panel audio line out connector.
- With jumpers removed, the connector provides audio line out and mic in signals for front panel audio connectors.

Table 18 describes the two configurations of this connector/jumper block.



CAUTION

Do not place jumpers on this block in any configuration other than the one described in Table 18. Other jumper configurations are not supported and could damage the Desktop Board.

Table 18. Front Panel Audio Connector/Jumper Block

Jumper Setting	Configuration
<p>5 and 6 9 and 10</p>	Audio line out signals are routed to the back panel audio line out connector.
<p>No jumpers installed</p>	Audio line out and mic in signals are available for front panel audio connectors.






INTEGRATOR'S NOTE

When the jumpers are removed and this connector is used for front panel audio, the back panel audio line out and mic in connectors are disabled.

2.3.2 BIOS SETUP CONFIGURATION JUMPER BLOCK

The 3-pin jumper block determines the BIOS Setup program's mode. Table 18A describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configuration mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

Table 18A. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

9. Change to Section 4.3, Main Menu, BIOS Setup Program

Section 4.3, Main Menu of the BIOS setup program will change in its entirety as follows:

4.3 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
-------------	-------------	----------	----------	-------	------	------

Table 26 describes the Main menu. This menu reports processor, memory, and Desktop Management Interface (DMI) information and is for configuring the system date and system time.

Table 26. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
System Bus Speed	No options	Displays the system bus speed.
System Memory Speed	No options	Displays the system memory speed.
Cache RAM	No options	Displays the size of second-level cache.
Total Memory	No options	Displays the total amount of RAM.
Memory Bank 0 Memory Bank 1	No options	Displays the amount and type of RAM in the memory banks.

continued

Table 26. Main Menu (continued)

Feature	Options	Description
Language	<ul style="list-style-type: none">• English (default)• Español	Selects the current default language used by the BIOS.
▶ Additional System Information	<ul style="list-style-type: none">• No options	Displays the system DMI Information
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of week Month/day/year	Specifies the current date.

Note: BIOS revision LY84510A.86A.0040.P16 or later is needed to support the *Additional System Information* submenu.

ERRATA

1. *Intel® 82801DB I/O Controller Hub 4 (ICH 4) Erratum 7*

PROBLEM: For a complete description of the ICH 4 erratum 7, see the Intel® 82801DB I/O Controller Hub 4 (ICH 4) Specification Update, order number 290745 found at <http://developer.intel.com/design/chipsets/specupdt>.

IMPLICATION: For a complete description of the ICH 4 erratum 7, see the Intel 82801DB I/O Controller Hub 4 (ICH 4) Specification Update, order number 290745 found at <http://developer.intel.com/design/chipsets/specupdt>.

WORKAROUND: None.

STATUS: This erratum was fixed in the B0 chipset stepping.

2. *Wake From an ACPI Sleep State Using Wake Methodologies May Fail*

PROBLEM: The desktop board hardware leaves the LAN RESET (LAN_RST#) signal unasserted before and after the resume well power (VccSus3_3 and VccSus1_5) is valid, instead of asserting it for 10 ms after valid power, which is required by the Intel 82801DB I/O Controller Hub 4 (ICH4) Datasheet (order number 290744). The result is that LAN wake attempts may fail.

NOTE: Wake from LAN* using the MagicPacket* utility will not be affected by this errata.

IMPLICATION: Users that take advantage of LAN wake methods to wake systems from an ACPI sleep state may experience some wake failures.

WORKAROUND: None.

STATUS: This issue was fixed in BIOS revision LY84510A.86A.0012.P06.

3. *Intel 82801DB I/O Controller Hub 4 (ICH 4) Erratum 8*

PROBLEM: For a complete description of the ICH 4 erratum 8, see the Intel 82801DB I/O Controller Hub 4 (ICH 4) Specification Update, order number 290745 found at <http://developer.intel.com/design/chipsets/specupdt>.

IMPLICATION: For a complete description of the ICH 4 erratum 8, see the Intel 82801DB I/O Controller Hub 4 (ICH 4) Specification Update, order number 290745 found at <http://developer.intel.com/design/chipsets/specupdt>.

WORKAROUND: None.

STATUS: This erratum may be fixed in a future chipset stepping.



4. *Supervisor Password Cleared When 256MB or Greater System Memory is Used*

PROBLEM: If 256MB or more system memory is added to a system the Supervisor password is cleared.

IMPLICATION: Supervisor password cannot be used with 256MB or more of system memory.

WORKAROUND: None.

STATUS: This erratum may be fixed in a future BIOS revision.

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *Technical Product Specification for Intel® Desktop Boards using the Intel® 845GL Chipset* (Order Number A90788). All Specification Clarifications will be incorporated into a future version of that specification.

1. **Change to Description of Table 4A, Section 2.2.2.2, Audio, Power, and Hardware Control Connectors**

Table 4A will be added to Section 2.2.2.2, Audio, Power, and Hardware Control Connectors as follows:

Table 4A. Front Panel Audio Connector

Pin	Signal Name	Pin	Signal Name
1	MIC_IN	2	Ground
3	MIC_BIAS	4	+5 V
5	RIGHT_OUT	6	RIGHT_IN
7	Not Connected	8	Key
9	LEFT_OUT	10	LEFT_IN

2. **Clarification of SMBus Routing**

Section 2.8.2.1 will change in its entirety as follows:

2.8.2.1 **Expansion Slots**

The Desktop Board has four PCI rev 2.2 compliant local bus slots. The SMBus is routed to PCI bus connector 2.

NOTE

The SMBus routing to the PCI bus connectors does not conform to the PCI Engineering Change Notice (ECN) “Addition of the SMBus to the PCI Connector ECN”, dated October 5th, 2000. The ECN specifies that SMBus signals must be routed to all PCI bus connectors. On this board, SMBus signals are routed to PCI bus connector 2 only.

Add-in cards that implement PCI bus connector pins A40 and A41 for any purpose other than SMBCLK (SMBus clock) and SMBDAT (SMBus data) should not be installed in PCI bus connector 2.

For information about**Refer to**

Addition of the SMBus to the PCI Connector ECN

http://www.pcisig.com/data/specifications/smb_ecn_040501.pdf **NOTE**

This document references back-panel slot numbering with respect to processor location on the Desktop Board. PCI slots are identified as PCI slot #x, starting with the slot closest to the processor. The ATX/microATX specifications identify expansion slot locations with respect to the far edge of a full-sized ATX chassis. The ATX specification and the Desktop Board's silkscreen are opposite and could cause confusion. The ATX numbering convention is made without respect to slot type, but refers to an actual slot location on a chassis. Figure 4 on page 18 illustrates the Desktop Board's PCI slot numbering.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Technical Product Specification for Intel® Desktop Boards using the Intel® 845GL Chipset* (Order Number A90788). All Documentation Changes will be incorporated into a future version of that specification.

1. **Change to Description of Section 3.8.2, Network Boot**

The following note will be added to Section 3.8.2, Network Boot:

INTEGRATOR'S NOTE

The F12 key may be disabled during POST by assigning a Supervisor Password and setting the User Access Level to a value other than Full.

For information about	Refer to
Supervisor Password and User Access Level	Section 4.5, page 68

2. **Change to Description of Section 3.8.4, Changing the Default Boot Device During POST**

The following note will be added to Section 3.8.4, Changing the Default Boot Device During POST:

INTEGRATOR'S NOTE

The F10 key may be disabled during POST by assigning a Supervisor Password and setting the User Access Level to a value other than Full.

For information about	Refer to
Supervisor Password and User Access Level	Section 4.5, page 68

3. **Removed Note That Specifies USB 2.0 Support Limited to Windows* 2000 and Windows XP From Section 1.7.2, USB**

The following note will be removed in its entirety from Section 1.7.2, USB:

NOTE

USB 2.0 support has been tested with Windows 2000 and Windows XP drivers and is not currently supported by any other operating system.



4. Removed ESCD Format Reference From Section 3.3.1, PCI Autoconfiguration

Remove the sentence "Autoconfiguration information is stored in ESCD format" from Section 3.3.1, PCI Autoconfiguration.

5. Add Alert Standard Format Specification Version 1.03 Dated June 20, 2001 to Section 1.4, Design Specifications

The following specification will be added to table 2, Section 1.4, Design Specifications:

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from...
ASF	<i>Alert Standard Format Specification</i>	Version 1.03, June 20, 2001, Distributed Management Task Force (DMTF).	http://www.dmtf.org/standards/documents/ASF/DSP0114.pdf